David Page

Senior FPGA Designer

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Profile

Dynamic, motivated, versatile and resourceful FPGA Designer with a Bachelor's degree in Electrical Engineering and a minor in Computer Science, adept at continual learning and skill development. Extensive experience spanning over 12 years in FPGA design including video processing, high-speed interfaces, algorithm research and translation from software to hardware. Proven ability to develop, debug, and simulate complex FPGA designs. Proficient in programming languages including Bash, Python, C/C++, VHDL, and SystemVerilog.

Through my career I learned to be adaptive to new technologies by reading and understanding what I do. I know the tradeoffs that hardware design requires. I am passionate about what I'm doing, I have expertise in multiple aspects of FPGA design such as High Speed communication protocols, SystemVerilog, Verification, and algorithm development on FPGA.

I embrace a philosophy of continual learning, reading and understanding new software, method or technology is part of who I am.

I have strong interest about Web3, Blockchain, Zero-Knowledge Proof, Algorithm development on hardware, Hardware Security, Cryptography and Autonomous Driving.

Summary

- More than 12 years of strong experience in FPGA design and verification flow. Architecture, RTL Coding, Verification, Synthesis, Static timing analysis, New board bring-up.
- Experience with ressource allocation, floorplanning, high speed protocol, constraints declaration.
- Experience with board design using Altera/Intel Arria5 and Arria10.
- Experience with algorithm development on FPGA from C model.
- Experience with multiple DSP configurations to achieve goals, fixed point and floating point operation.
- Personal project experience using Vivado 2023, Xilinx/AMD SoC, Vivado Block Design, AXI buses, PS-PL project, DMA Simulation.
- Strong knowledge of ModelSim simulation tool, UVM simulation in SystemVerilog.
- Proficient with C/C++, VHDL, Verilog, SystemVerilog, Python, Bash, Linux, Tcl.
- Experience with multiple protocols such as DisplayPort, HDMI, SDI, Interlaken.
- Proficient in real lab debugging using logic analyzer, oscilloscope and other tools.
- Pragmatic approach to problems.

Technical Skills

Knowledge of the following tools and language:

- VHDL, Verilog, SystemVerilog, UVM, Vivado, Quartus, ModelSim, TimeQuest, ILA, SignalTap, DisplayPort, HDMI, Interlaken, MATLAB.

Professional Experience

FPGA Designer

VPixx Technologies Inc.

2016 - Present

Product owner and head of R&D of an eye tracker device.

Achievements + Highlights

- Lead FPGA Designer for a computer vision algorithm project:
  - Responsible for the research on how to optimize the algorithm
  - Responsible of maintaining all code including the C model and the VHDL
  - Responsible of all FPGA workflow and simulation
- Developped and maintained a UVM SystemVerilog verification environment to validate all major products which helped solved many corner case bugs before they arrived at the client.
- Bring up of major product lines
- High Speed interface communication protocol design: CMOS, DisplayPort, Optical fiber via Interlaken communication between multiple FPGA devices.

FPGA Designer

Matrox Electronic Sytems

2011 - 2015

- Worked on multiple PCI-Express video accelerator board.
- Specialized in video processing in FPGA, focusing on pipelining, design, debug, and simulation.
- Successfully contributed to the development and enhancement of video processing algorithms.
- Demonstrated proficiency in FPGA design methodologies and best practices.
- Worked on different modules such as DMA, video scaler, video blender, DDR interface/arbiter.

Education

Electrical Engineering with a minor in computer science

Université du Québec à Trois-Rivières// Trois-Rivières, Qc // 2010

Skills + interests

Computer // Programming // Linux // Embedded // Security // Research // Reading // Web3 // Art // Photography // Travel // Continuous learning // Speaks French & English